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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/729,401	12/05/2003	Gary L. Swoboda	TI-34667	9599

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EXAMINER

FENNEMA, ROBERT E

ART UNIT	PAPER NUMBER
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2183

DATE MAILED: 09/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/729,401	<b>Applicant(s)</b> SWOBODA ET AL.	
	<b>Examiner</b> Robert E. Fennema	<b>Art Unit</b> 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 05 December 2003.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

1. Claims 1-11 are pending.

#### ***Claim Objections***

2. Claims 1 and 9 are objected to for referring to "the" pipeline flattener, when no pipeline flattener has been introduced at these points. It has been assumed throughout the rest of this Office Action that the claims read "a" flattener.

#### ***Claim Rejections - 35 USC § 101***

3. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claim 6 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claim 6 discloses transmitting a plurality of trace streams to a host processor, and a marker signal group in a different trace stream, which has a variety of attributes. However, this claim is non-statutory, as it is claiming the transmission of data which may or may not have a tangible result when received, and is claiming a signal with attributes, which also has no tangible result, as it is not used anywhere in the target or host processor, and a signal is not statutory subject matter. In addition, the transmission occurs in the preamble of the claim, which is not given patentable weight.

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim 6 is rejected under 35 U.S.C. 102(b) as being anticipated by Bridges et al. (USPN 5,809,293, herein Bridges).

7. As per Claim 6, Bridges teaches: In a processing unit test environment wherein a target processor transmits a plurality of trace streams to a host processing unit, a program code start point sync marker signal group in a trace signal stream, the marker signal group comprising:

indicia of the occurrence of a program code start point signal (Column 8, Lines 49-51);

indicia of the relationship of the occurrence of the program code start point signal to the target processor clock (Column 7, Lines 30-33); and

indicia of the relationship of the occurrence of the program code start point signal to the target processor program execution (Column 2, Lines 49-51).

***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 1-3 and 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bridges, in view of Official Notice.

10. As per Claim 1, Bridges teaches: During the testing of the operation of processing unit, a system for identifying the occurrence of a program code start point condition in the pipeline flattener, the system comprising:

program counter trace apparatus responsive to signals from the processing unit, the program counter trace apparatus generating a program counter trace stream (Column 4, Lines 31-34, the program counter outputs the PC, which can be traced, in combination with Column 6, Lines 34-44, the Event Detection Unit, which performs the functions of the program counter trace apparatus described below); and

synchronization apparatus applying periodic signals to the timing trace apparatus and to the program counter trace apparatus, the periodic signals resulting in periodic sync markers in the timing trace stream and in the program counter trace stream (Column 6, Lines 34-44, the event detection circuit can detect a trace condition and send out a signal indicating as such).

wherein the program counter trace apparatus is responsive to a program code start point signal, the program counter trace apparatus generating a sync marker signal group identifying the occurrence of the program code start point signal and relating the beginning of program code execution to the timing trace stream and to the program

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code execution (Column 6, Lines 34-44, in recognition of the trace event, a signal is generated, which indicates the start the trace), but fails to teach:

timing trace apparatus responsive to signals from the processor unit, the timing trace apparatus generating a timing trace stream.

While Bridges does not teach a timing trace apparatus, Bridges does teach that various clock signals exist in his system, but they are not shown due to being well-known in the art (Column 7, Lines 30-33). A clock represents timing in the system, and Examiner is taking official notice that a clock signal is a well-known object to output to a trace system in order to determine how the system is functioning, and that one of ordinary skill in the art would have been motivated and able to output this clock signal with the other data. Further evidence to this effect can be seen in Bridges, Column 7, Lines 2-7, which says that information necessary to allow a user to determine a sequence of instructions is collected.

11. As per Claim 2, Bridges teaches: The system as recited in claim 1 wherein the marker signal group includes a program counter address (Column 22, Lines 49-51), a timing index (See Claim 1 for why the timing would have been included as well) and a periodic sync ID (Column 2, Lines 48-51).

12. As per Claim 3, Bridges teaches: The system as recited in claim 1 further comprising:

data trace apparatus responsive to signals from the processing unit, the data trace apparatus generating a data trace stream (Column 2, Lines 31-39, the FIFO queue holds data to create data traces to send to a host), wherein the periodic signals are applied to the data trace apparatus resulting in periodic sync markers in the data trace stream (Column 2, Lines 48-55, the registers which are traced result in periodic markers of the data trace); and

a host processing unit, the host processing unit responsive to the timing trace stream, the program counter trace stream and the data trace stream, the host processing unit reconstructing the processing activity of the processing unit from the trace streams (Column 3, Lines 9-14).

13. As per Claim 7, Bridges teaches: In a target processing unit generating trace test signals for transfer to a host processing unit, a program counter trace generation apparatus comprising:

sync marker assembly apparatus, the sync marker assembly apparatus including:

a storage unit (Column 2, Lines 49-51, the FIFO queue);

a decoder unit responsive to a program code start point signal for storing an indicia of the program code start point signal in the storage unit, the decoder unit generating a control signal (Figure 1, Event Detection 106. When it determines the event has occurred, a control signal is sent out which stores the program code start

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point in the registers, which then goes to the FIFO (Column 2, Lines 49-51, and Column 6, Lines 34-56);

a gate unit having a periodic sync signal (Column 4, Lines 27-30), and a program counter address (Column 4, Lines 31-34), the gate unit storing the periodic sync signal and the program counter address in the storage unit in response to the control signal (Column 6, Lines 34-56); and

a FIFO unit, the storage unit transferring the stored signals to the FIFO unit in the form of a program code start point sync marker (Column 2, Lines 31-40), but fails to teach:

a gate unit having a timing index; and

the gate unit storing the timing index.

While Bridges does not teach tracing the timing and storing that timing in a gate unit, Bridges does teach that various clock signals exist in his system, but they are not shown due to being well-known in the art (Column 7, Lines 30-33). A clock represents timing in the system, and Examiner is taking official notice that a clock signal is a well-known object to output to a trace system in order to determine how the system is functioning, and that one of ordinary skill in the art would have been motivated and able to output this clock signal with the other data, requiring it to be stored in a fashion similar to the other data sent to the FIFO. Further evidence to this effect can be seen in Bridges, Column 7, Lines 2-7, which says that information necessary to allow a user to determine a sequence of instructions is collected.



14. As per Claim 8, Bridges teaches: The program counter trace apparatus as recited in claim 7 responsive to a selected control signal for transferring the program code start point sync marker in the FIFO unit to an output port of the target processor (Column 8, Lines 60-65).

15. As per Claim 9, Bridges teaches: The program counter trace apparatus as recited in claim 8 wherein the apparatus can form a periodic sync marker in response to a periodic sync signal (Column 2, Lines 48-51).

16. Claims 4-5 and 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bridges and Official Notice, further in view of Alpert et al. (USPN 5,659,679).

17. As per Claim 4, Bridges teaches: The method for communicating an occurrence of a program code start point signal from a target processor unit to a host processing unit (Column 3, Lines 9-14), the method comprising:

a program counter trace stream (Column 4, Lines 31-34, the program counter outputs the PC, which can be traced, in combination with Column 6, Lines 34-44, the Event Detection Unit), and data trace stream (Column 2, Lines 31-39, the FIFO queue holds data to create data traces to send to a host), and

in the program counter trace stream, including a program code start point sync marker signal group indicating an occurrence of a program code start point signal and relating the signal occurrence to the data trace stream and to the timing trace stream

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(Column 6, Lines 34-44, in recognition of the trace event, a signal is generated, which indicates the start the trace, causing the streams to be stored), but fails to teach:

generating a timing trace stream;

While Bridges does not teach tracing the timing, Bridges does teach that various clock signals exist in his system, but they are not shown due to being well-known in the art (Column 7, Lines 30-33). A clock represents timing in the system, and Examiner is taking official notice that a clock signal is a well-known object to output to a trace system in order to determine how the system is functioning, and that one of ordinary skill in the art would have been motivated and able to output this clock signal with the other data. Further evidence to this effect can be seen in Bridges, Column 7, Lines 2-7, which says that information necessary to allow a user to determine a sequence of instructions is collected. However, this combination still fails to teach:

after return from an interrupt service routine.

While Bridges teaches tracing data on breakpoints chosen by the user, he does not explicitly teach that one of the breakpoints chosen by the user could be a change from a first instruction code sequence to a second instruction code sequence. However, Alpert teaches that one type of event that is favorable to trace is a return from a jump, that is, a change in the flow of execution (Abstract, and Column 4, Lines 42-50, and a return from an interrupt is a change in flow), in order to "profile" the code to determine bottlenecks (Column 2, Lines 46-66). Given that Bridges teaches that the user can select any event to begin a trace, and that Alpert teaches that a change in instruction flow is worth tracing, in order to profile, one of ordinary skill in the art at the time the

invention was made would have been motivated to use Alpert's teachings to trigger a trace in Bridge's invention on a jump or other similar instruction flow change.

18. As per Claim 5, Bridges teaches: The method as recited in claim 4 further including:

including periodic sync markers in the timing trace stream and in the program counter trace stream (Column 4, Lines 27-30 and Column 2, Lines 48-49); and

19. including in the program code sync marker reference to a periodic sync marker (Column 2, Lines 48-51).

20. As per Claim 10, Bridges teaches: The program counter trace apparatus as recited in claim 9, but fails to teach:

wherein the program code start point signal indicates the change from a first instruction code sequence to a second instruction code sequence exiting the pipeline flattener.

While Bridges teaches tracing data on breakpoints chosen by the user, he does not explicitly teach that one of the breakpoints chosen by the user could be a change from a first instruction code sequence to a second instruction code sequence. However, Alpert teaches that one type of event that is favorable to trace is a return from a jump, that is, a change in the flow of execution (Abstract), in order to "profile" the code to determine bottlenecks (Column 2, Lines 46-66). Given that Bridges teaches that the user can select any event to begin a trace, and that Alpert teaches that a change in

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instruction flow is worth tracing, in order to profile, one of ordinary skill in the art at the time the invention was made would have been motivated to use Alpert's teachings to trigger a trace in Bridge's invention on a jump or other similar instruction flow change.

21. As per Claim 11, Alpert teaches: The program counter trace apparatus as recited in claim 10 wherein the first instruction code sequence is an interrupt service routine code and the second instruction sequence is a program code (Column 4, Lines 42-50, a return from an interrupt is a change in execution flow and functions like a jump).

### ***Conclusion***

22. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

23. Ball (USPN 5,615,357) teaches a tracing system tracing similar data to the applicant.

24. Flores et al. (USPN 6,889,311) teaches a tracing system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert E. Fennema whose telephone number is (571) 272-2748. The examiner can normally be reached on Monday-Friday, 8:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Robert E Fennema  
Examiner  
Art Unit 2183

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